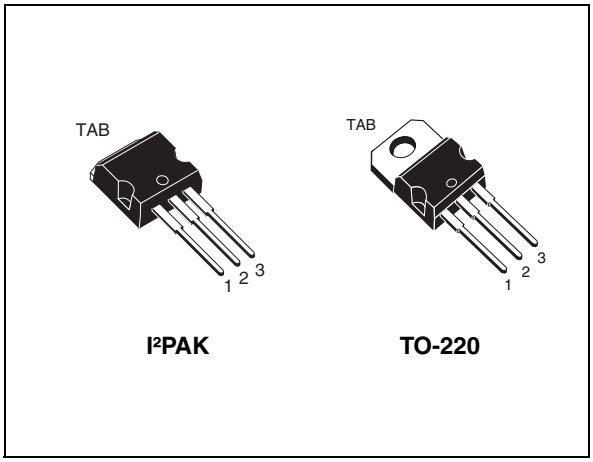
STI260N6F6
STP260N6F6

N-channel 60 V, 0.0024 Ω, 120 A STripFET™ VI DeepGATE™ Power MOSFET in TO-220 and I²PAK packages

Features

Order codes	V_{DSS}	$R_{DS(on)}$ max	I_D
STI260N6F6 STP260N6F6	60 V	< 0.003 Ω	120 A

- Low gate charge
- Very low on-resistance
- High avalanche ruggedness



Application

- Switching applications

Description

These devices are N-channel Power MOSFETs developed using the 6th generation of STripFET™ DeepGATE™ technology, with a new gate structure. The resulting Power MOSFETs exhibits the lowest $R_{DS(on)}$ in all packages.

Figure 1. Internal schematic diagram

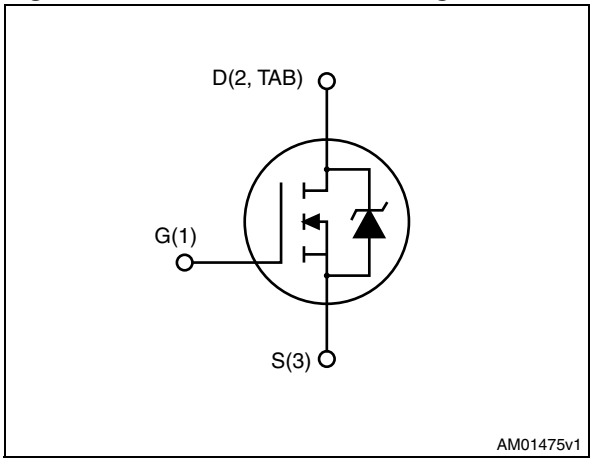


Table 1. Device summary

Order codes	Marking	Package	Packaging
STI260N6F6	260N6F6	I²PAK	Tube
STP260N6F6		TO-220	

Contents

1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	60	V
V_{GS}	Gate-source voltage	± 20	V
I_D	Drain current (continuous) at T_C = 25 °C	120	A
I_D	Drain current (continuous) at T_C = 100 °C	120	A
I_{DM} (1)	Drain current (pulsed)	480	A
P_{TOT}	Total dissipation at T_C = 25 °C	300	W
	Derating factor	2	W/°C
T_{stg}	Storage temperature	- 55 to 175	°C
T_j	Operating junction temperature		

1. Current limited by package.

Table 3. Thermal data

Symbol	Parameter	Value	Unit
$R_{thj\text{-}case}$	Thermal resistance junction-case max	0.5	°C/W
$R_{thj\text{-}a}$	Thermal resistance junction-ambient max	62.5	°C/W
T_l	Maximum lead temperature for soldering purpose	300	°C

2 Electrical characteristics

(T_{CASE} = 25 °C unless otherwise specified)

Table 4. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage (V_{GS} = 0)	I_D = 250 µA	60			V
I_{DSS}	Zero gate voltage Drain current (V_{GS} = 0)	V_{DS} = 60 V V_{DS} = 60 V, T_C=125 °C			1 100	µA µA
I_{GSS}	Gate-body leakage current (V_{DS} = 0)	V_{GS} = ± 20 V			± 100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 250 µA	2		4	V
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS} = 10 V, I_D = 60 A		2.4	3	mΩ

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{DS} = 25 V, f = 1 MHz, V_{GS} = 0	-	11400	-	pF
C_{oss}	Output capacitance			850		pF
C_{rss}	Reverse transfer capacitance			368		pF
Q_g	Total gate charge	V_{DD} = 30 V, I_D = 120 A, V_{GS} = 10 V *(see Figure 14)*	-	183	-	nC
Q_{gs}	Gate-source charge			53		nC
Q_{gd}	Gate-drain charge			41		nC

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD} = 30 V, I_D = 60 A R_G = 4.7 Ω V_{GS} = 10 V *(see Figure 13)*	-	31.4	-	ns
t_r	Rise time			165		ns
$t_{d(off)}$	Turn-off-delay time		-	144.4	-	ns
t_f	Fall time			62.6		ns

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max	Unit
I_{SD}	Source-drain current		-		120	A
I_{SDM} (1)	Source-drain current (pulsed)		-		480	A
V_{SD} (2)	Forward on voltage	I_{SD} = 120 A, V_{GS} = 0	-		1.1	V
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	I_{SD} = 120 A, V_{DD} = 48 V di/dt = 100 A/µs, T_j = 150 °C *(see Figure 15)*	-	55.6 116 3.8		ns nC A

1. Current limited by package.
2. Pulsed: pulse duration = 300 µs, duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

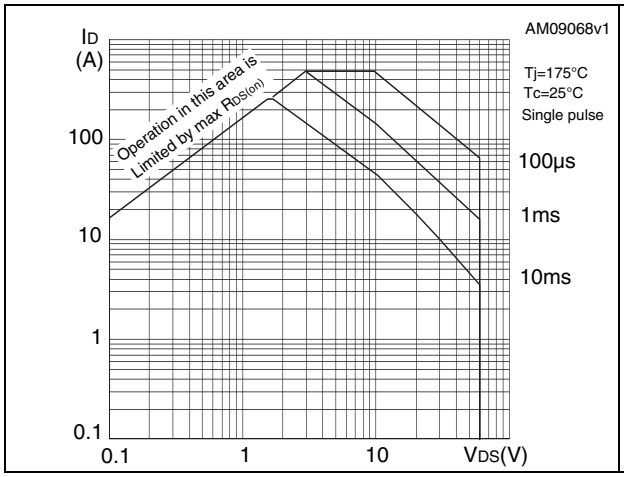


Figure 3. Thermal impedance

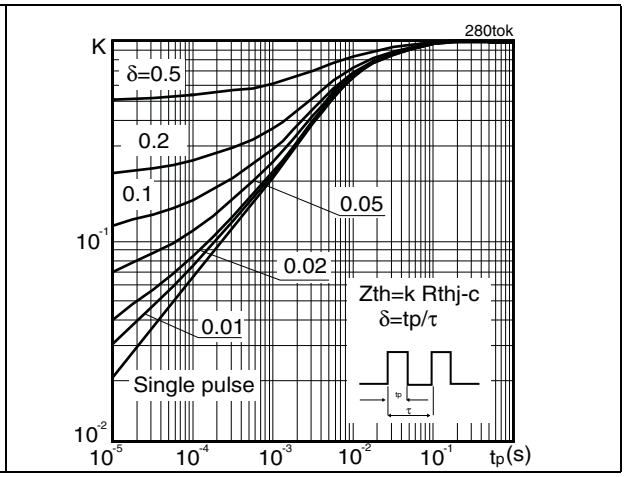


Figure 4. Output characteristics

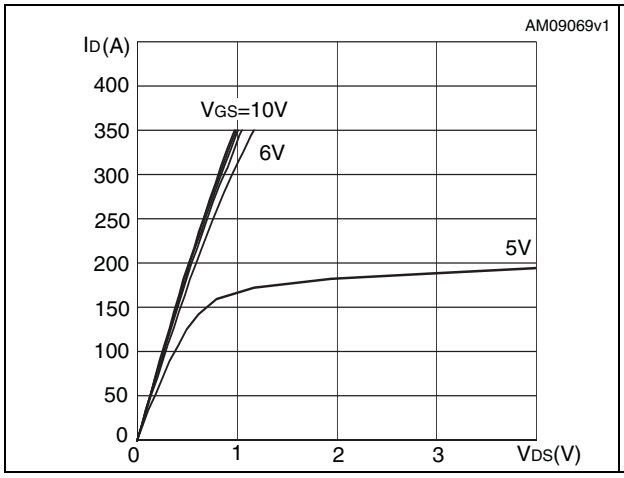


Figure 5. Transfer characteristics

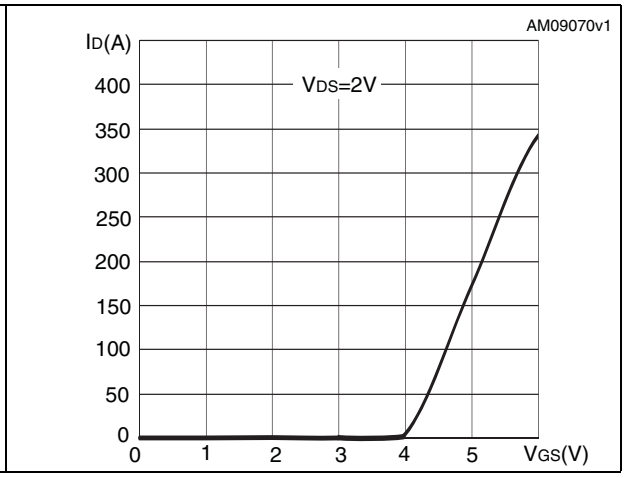


Figure 6. Normalized B_{VDSS} vs. temperature

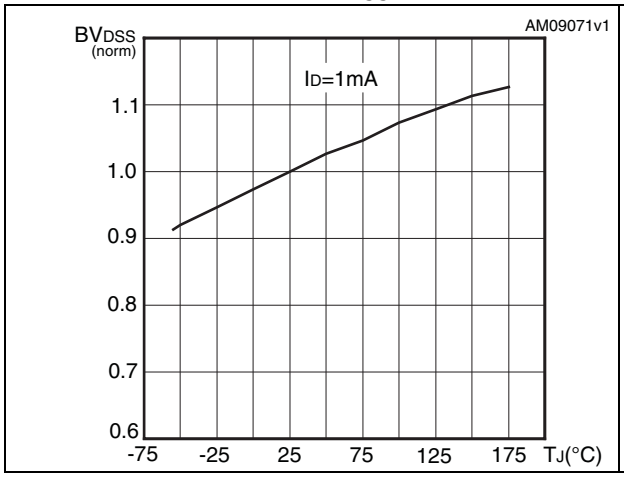


Figure 7. Static drain-source on resistance

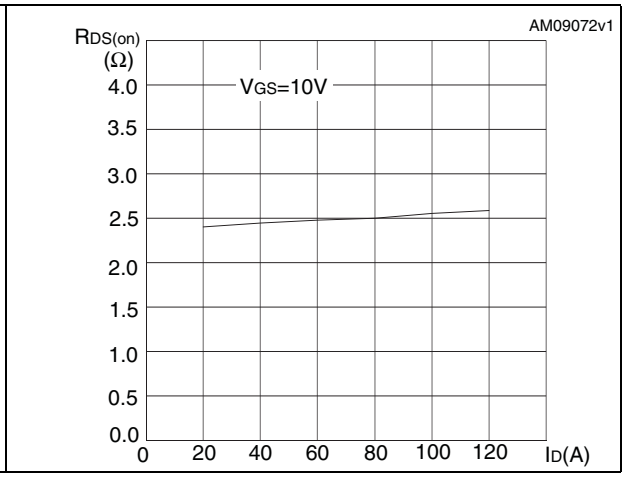


Figure 8. Gate charge vs. gate-source voltage

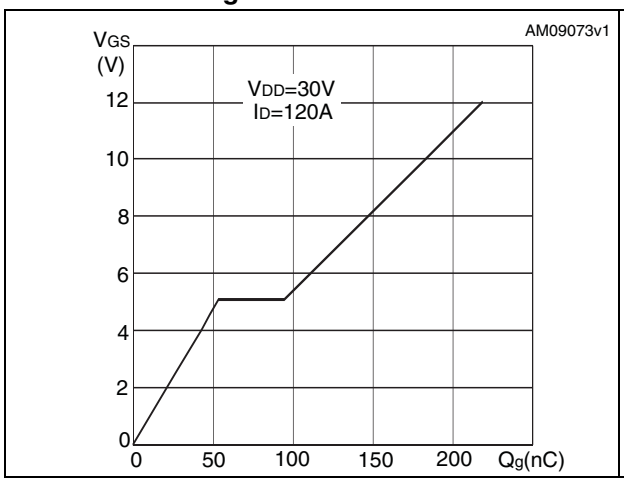


Figure 9. Capacitance variations

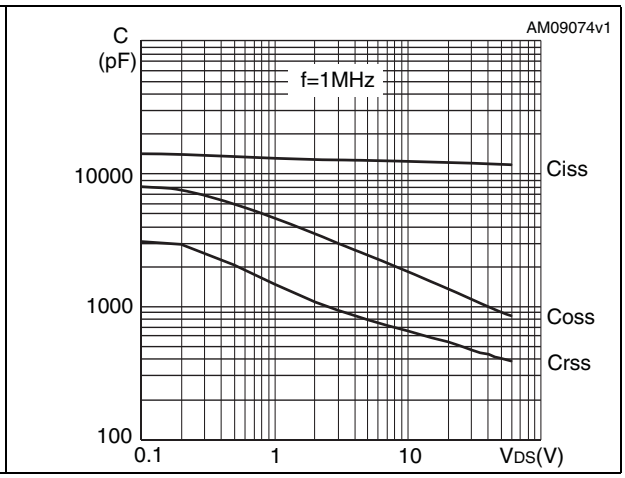


Figure 10. Normalized gate threshold voltage vs. temperature

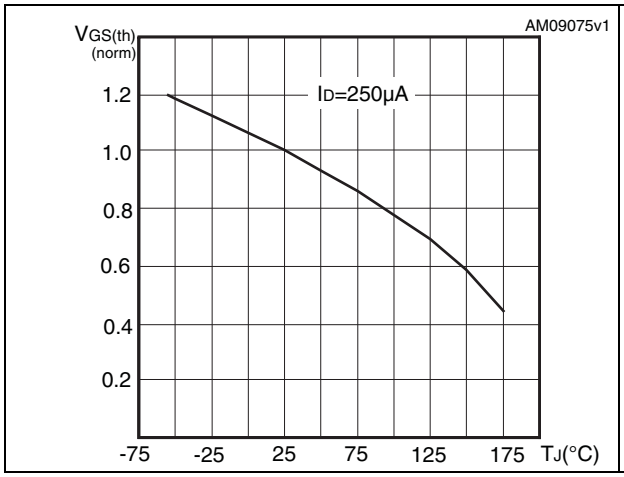


Figure 11. Normalized on resistance vs. temperature

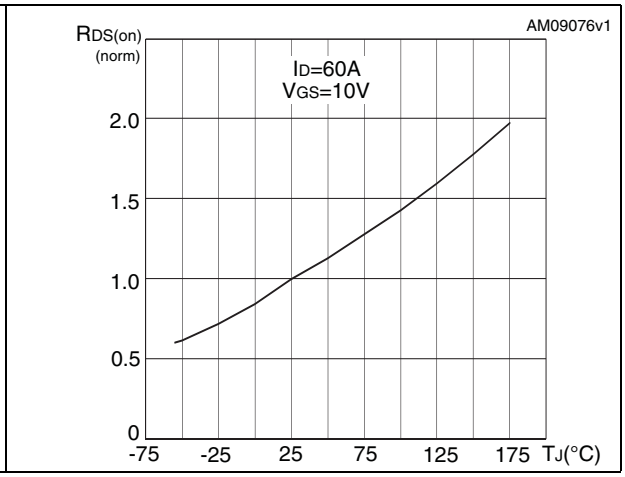
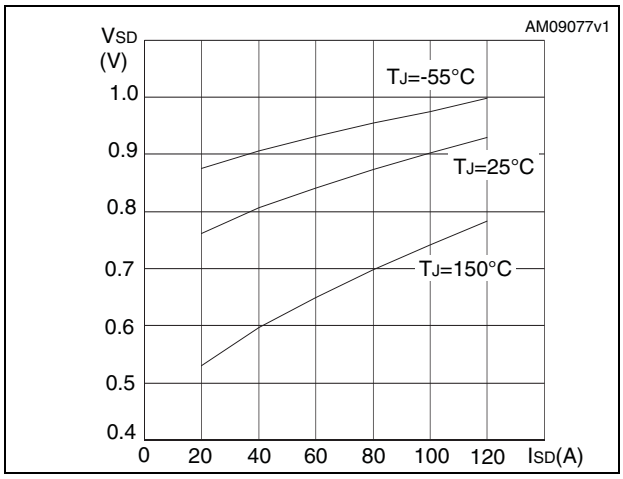


Figure 12. Source-drain diode forward characteristics



3 Test circuits

Figure 13. Switching times test circuit for resistive load

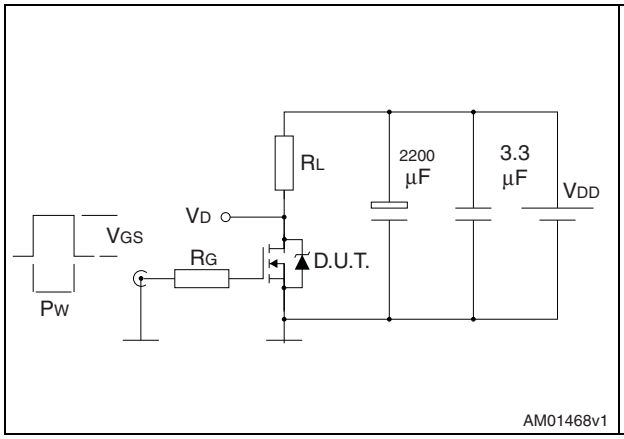


Figure 14. Gate charge test circuit

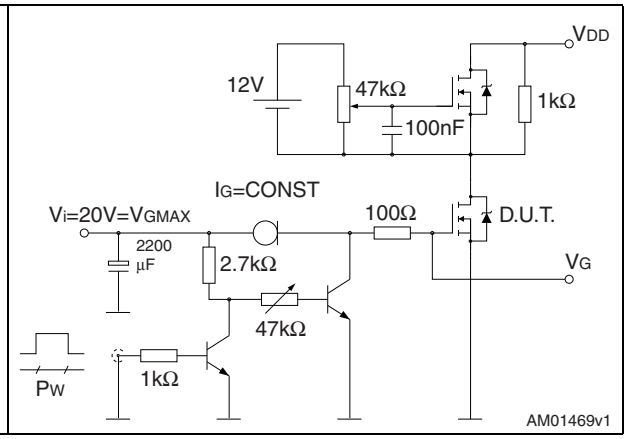


Figure 15. Test circuit for inductive load switching and diode recovery times

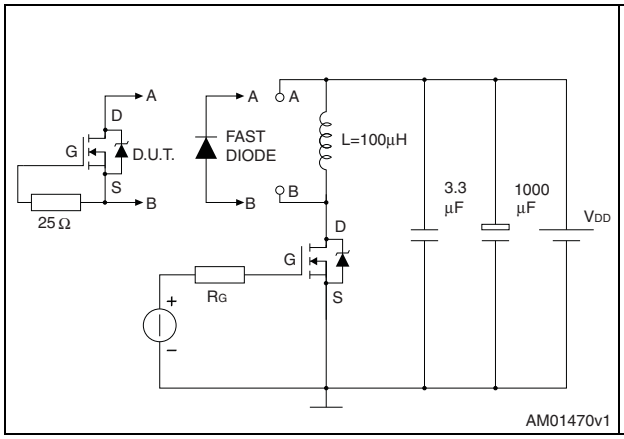


Figure 16. Unclamped inductive load test circuit

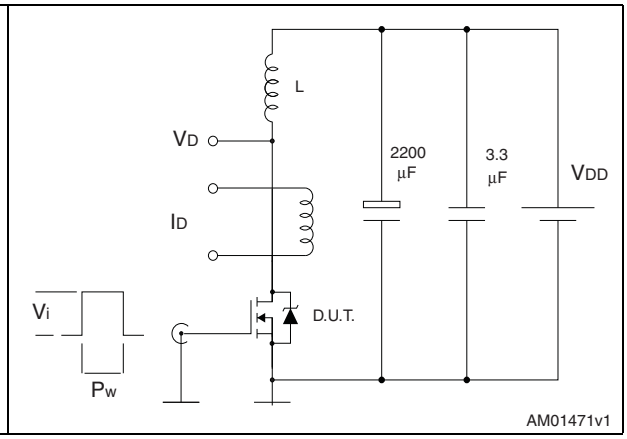


Figure 17. Unclamped inductive waveform

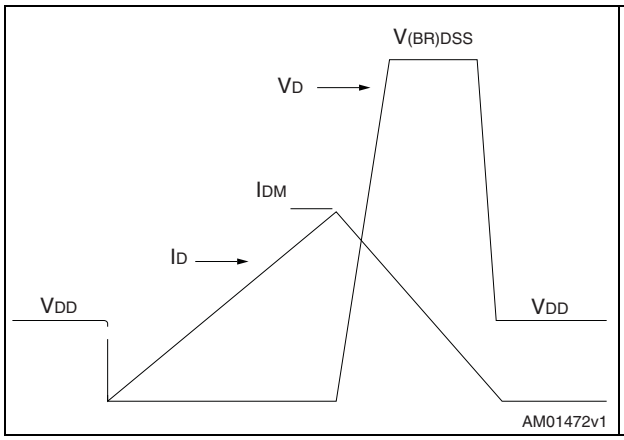
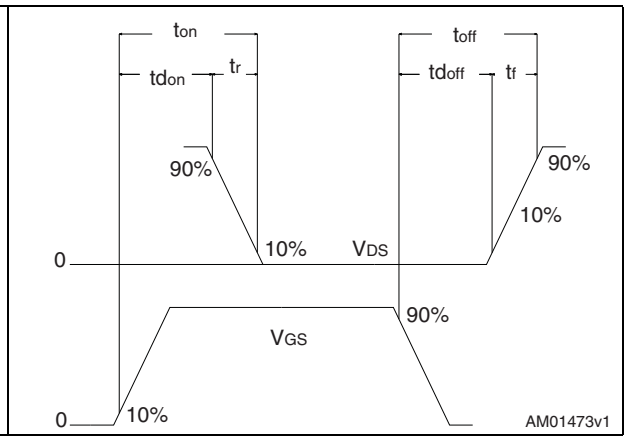


Figure 18. Switching time waveform



4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

Table 8. I²PAK (TO-262) mechanical data

DIM.	mm.		
	min.	typ	max.
A	4.40		4.60
A1	2.40		2.72
b	0.61		0.88
b1	1.14		1.70
c	0.49		0.70
c2	1.23		1.32
D	8.95		9.35
e	2.40		2.70
e1	4.95		5.15
E	10		10.40
L	13		14
L1	3.50		3.93
L2	1.27		1.40

Figure 19. I²PAK (TO-262) drawing

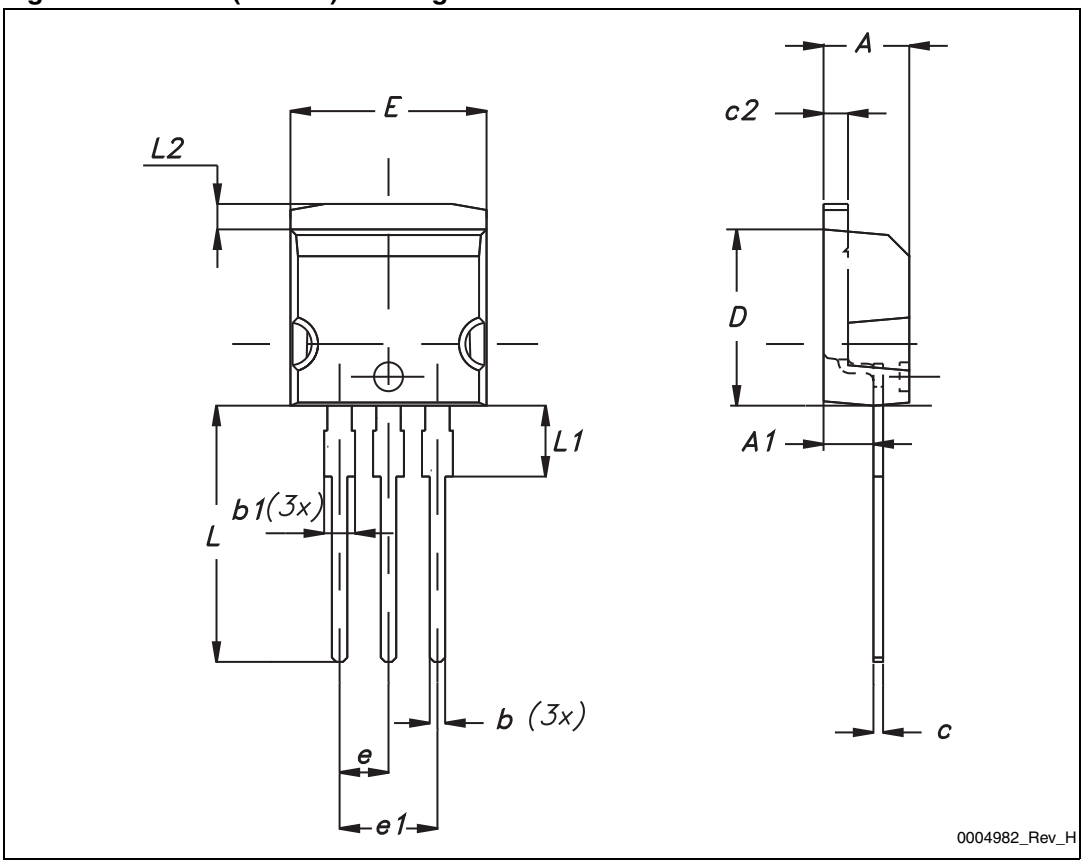
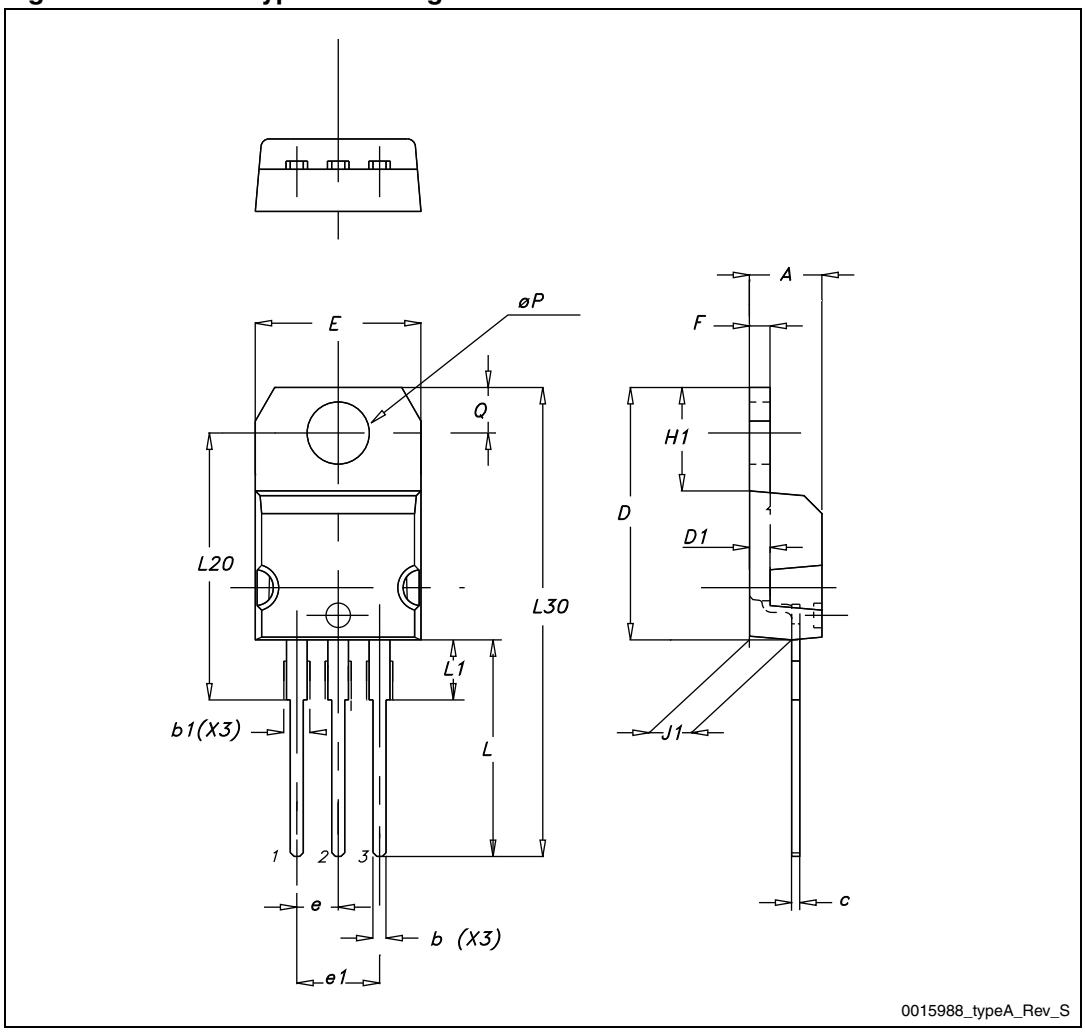


Table 9. TO-220 type A mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
b	0.61		0.88
b1	1.14		1.70
c	0.48		0.70
D	15.25		15.75
D1		1.27	
E	10		10.40
e	2.40		2.70
e1	4.95		5.15
F	1.23		1.32
H1	6.20		6.60
J1	2.40		2.72
L	13		14
L1	3.50		3.93
L20		16.40	
L30		28.90	
∅P	3.75		3.85
Q	2.65		2.95

Figure 20. TO-220 type A drawing



5 Revision history

Table 10. Document revision history

Date	Revision	Changes
07-May-2010	1	First release.
18-Apr-2011	2	Document status promoted from preliminary data to datasheet.
27-Apr-2011	3	*Device summary* has been updated.
05-Oct-2011	4	*Table 2: Absolute maximum ratings* has been updated. Minor text changes.
13-Jan-2012	5	Updated *Table 2: Absolute maximum ratings*.

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